



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 1901

| | | | | |
|-----------------------------|-----------------------------------|--------------|-------------------------------|---------------------------------|
| SERIAL NUMBER 10/647,217 | FILING DATE 08/26/2003 RULE | CLASS 714 | GROUP ART UNIT <i>2117</i> | ATTORNEY DOCKET NO. SON-2810 |
|-----------------------------|-----------------------------------|--------------|-------------------------------|---------------------------------|

APPLICANTS

Yoshitaka Kayukawa, Kanagawa, JAPAN;

DG

Tetsuya Aoki, Tokyo, JAPAN;

Takahiro Hamaguchi, Kanagawa, JAPAN; Noriyuki Oshima, Kanagawa, JAPAN;

** CONTINUING DATA *** *none*** FOREIGN APPLICATIONS *** *DG*
JAPAN P2002-277285 09/24/2002IF REQUIRED, FOREIGN FILING LICENSE GRANTED *DG*
** 11/22/2003

| | | | | | |
|--|--|---------------------------|---------------------|--------------------|-------------------------|
| Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no | 35 USC 119 (b-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance | STATE OR COUNTRY JAPAN | SHEETS DRAWING 4 | TOTAL CLAIMS 12 | INDEPENDENT CLAIMS 7 |
| Verifier and Acknowledged <i>DG</i> | Examiner's Signature <i>DG</i> Initials | | | | |

ADDRESS
 23353
 RADER FISHMAN & GRAUER PLLC
 LION BUILDING
 1233 20TH STREET N.W., SUITE 501
 WASHINGTON , DC
 20036

TITLE
 Semiconductor integrated circuit and method for testing same

| | | |
|------------|--|--|
| FILING FEE | FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT | <input type="checkbox"/> All Fees |
| | | <input type="checkbox"/> 1.16 Fees (Filing) |
| | | <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) |